CLAIMS

We claim:

1. A microsystem-on-a-chip, comprising:

a bottom chip comprising one or more microsystem devices with associated input/output pads on the top surface of the bottom chip;

an interconnect layer on the top surface of the bottom chip, the interconnect layer comprising a compliant dielectric material and an interconnect structure embedded in the compliant dielectric material, the interconnect structure comprising one or more via capture pads connected to the associated input/output pads on the top surface of the bottom chip; and

a thin upper chip on the interconnect layer, the thin upper chip comprising one or more microsystem devices with associated input/output pads on the top surface of the thin upper chip that are connected to the one or more via capture pads in the interconnect layer by conductive vias through the thin upper chip.

2. The microsystem-on-a-chip of Claim 1, further comprising at least one additional stacked layer on the thin chip, each additional stacked layer comprising:

a stacked interconnect layer on the top surface of the thin upper chip, the stacked interconnect layer comprising a compliant dielectric material and an interconnect structure embedded in the compliant dielectric material, the interconnect structure comprising one or more via capture pads connected to the associated input/output pads on the top surface of the thin upper chip; and

a stacked thin chip on the stacked interconnect layer, the stacked thin chip comprising one or more microsystem devices with associated input/output pads on the top surface of the stacked thin chip that are connected to the one or more via capture pads in the stacked interconnect layer by conductive vias through the stacked thin chip.

3. The microsystem-on-a-chip of Claim 1, wherein the interconnect layer has a thickness of less than 50 microns.

4. The microsystem-on-a-chip of Claim 1, wherein the compliant dielectric material is a polymer.

5. The microsystem-on-a-chip of Claim 4, wherein the polymer is benzocyclobutene.

6. The microsystem-on-a-chip of Claim 1, wherein the thin upper chip has a thickness of less than 120 microns.

7. The microsystem-on-a-chip of Claim 1, wherein the interconnect structure further comprises at least one passive component.

8. The microsystem-on-a-chip of Claim 7, wherein the embedded passive comprises a thin-film resistor.

9. The microsystem-on-a-chip of Claim 7, wherein the embedded passive comprises a multi-layer capacitor.

10. The microsystem-on-a-chip of Claim 7, wherein the embedded passive comprises a spiral inductor.

11. The microsystem-on-a-chip of Claim 1, wherein the interconnect structure comprises copper.

12. The microsystem-on-a-chip of Claim 1, wherein the on or more via capture pads are sized to control the alignment tolerance of the thin upper chip.

13. A method for fabricating a plurality of microsystems-on-a-chip, comprising:

providing a bottom wafer comprising a plurality of chips, each chip comprising one or more microsystem devices with associated input/output pads on the top surface of the bottom wafer;

forming an interconnect layer on the top surface of the bottom wafer, the interconnect layer comprising a compliant dielectric material and an interconnect structure embedded in the compliant dielectric material, the interconnect structure comprising one or more via capture pads connected to the associated input/output pads on the top surface of the bottom wafer;

bonding a thin upper wafer to the interconnect layer, the thin upper wafer comprising a plurality of chips, each chip comprising one or more microsystem devices with associated input/output pads on the top surface of the thin upper wafer that are connected to the one or more via capture pads in the interconnect layer by conductive vias through the thin upper wafer; and

singulating the plurality of chips from the bottom wafer, the interconnect layer and the thin wafer.

14. The method of Claim 13, further comprising:

forming hollow vias in the thin upper wafer prior to bonding the thin upper wafer to the interconnect layer;

etching the hollow vias through to the one or more via capture pads in the interconnect layer after bonding the thin upper wafer to the interconnect layer; and

metallizing the hollow vias to provide the conductive vias.

15. The method of Claim 13, further comprising:

forming hollow vias in the thin upper wafer through to the one or more via capture pads in the interconnect layer after bonding the thin upper wafer to the interconnect layer; and

metallizing the hollow vias to provide the conductive vias.

16. A method for aligned bonding of a thin upper wafer to a bottom wafer, comprising:

providing the bottom wafer;

depositing an interconnect layer on the top surface of the thick bottom wafer;

providing a thick upper wafer;

attaching a thick carrier wafer to the top surface of the thick upper wafer with a thermal release tape having a thermal release temperature;

thinning the bottom surface of the thick upper wafer to provide a thin upper wafer;

bonding the bottom surface of the thin upper wafer to the exposed surface of the interconnect layer; and

heating the bonded wafers to above the thermal release temperature to release the thermal release tape and the carrier wafer from the thin upper wafer.